This invention is submitted in the name of Inventor John McCollum, Assignor to Actel Corporation, a California Corporation.

SPECIFICATION

TRANSISTOR HAVING FULLY-DEPLETED JUNCTIONS

TO REDUCE CAPACITANCE AND INCREASE RADIATION

IMMUNITY IN AN INTEGRATED CIRCUIT

BACKGROUND

1. Field of the Invention

[0001]   The present invention relates to programmable switches in an integrated circuit. More specifically, the invention relates to reducing capacitance of a transistor junction to increase performance and speed in an integrated circuit and to increasing radiation immunity in integrated circuits.

2. Background

[0002]   Integrated circuits in general can benefit from lower junction capacitances of MOS transistors to improve switching speed. Integrated circuits can also benefit from by using transistors that have improved immunity to radiation. These benefits are desirable in both standard MOS transistors and floating-gate memory transistors.

[0003]   FPGA integrated circuits are known in the art. FPGAs may be classified in one of two categories.   One category of FPGAs employs programmable elements that are one-time programmable, such as antifuses for making programmable connections. The other category of FPGAs employs programmable elements that are re-programmable and uses transistor switches to make programmable connections.

[0004]   Typically, an FPGA has an array of logic elements and wiring interconnections with many thousands of programmable interconnect cells so that the FPGA can be configured by the user into an integrated circuit with defined functions. Each programmable interconnect cell, or switch, can connect two circuit nodes in the integrated circuit to make or break a wiring interconnection or to set the function or functions of a logic element.

[0005]   Reprogrammable FPGA devices include some means for storing program information used to control the programmable elements. Non-volatile memory devices such as EPROMs, EEPROMs, non-volatile RAM and flash memory devices have all been proposed for or used to store programming information in the class of FPGA applications.

[0006]   An ideal memory device optimizes density, preserves critical memory in a nonvolatile condition, is easy to program and reprogram, and is read

2

quickly. Some non-volatile memory devices meet more of the above requirements than others. For instance, EPROMS are high density, however, they have to be exposed to ultra-violet light for erasure. EEPROMS are electrically byte-erasable, but are less reliable and have the lowest density. Flash memory devices, however, are low-cost, high-density, low-power, high-reliability devices resulting in a high-speed architecture.

[0007]   Integrated circuits, notably memories, such as memory cells, are often used in environments where they are or may be subjected to high-energy particles. They may also be subjected to a high-energy electromagnetic pulse field. Such particles may include alpha, beta, gamma and other particles, which have sufficient energy to pass through the outer surface of a package and impact the memory cell itself.

[0008]   Outer space is one environment in which a memory cell would be subjected to impact from a high-energy particle. When the sun experiences an energy eruption, which occurs with increasing frequency and intensity during high activity sunspot cycles, the likelihood of impact of a high-energy particle on objects orbiting the earth becomes extremely high. Other environments, such as nuclear strike may also produce high-energy particles or a high-energy electromagnetic pulse (EMP).

[0009] Many integrated circuits in use today have a reversed-biased PN junction that is subject to short-circuiting due to charges generated by the high-energy particle hit. If this happens to a standard memory cell, the logic state of the cell becomes unknown. It may be inverted, or the data may be erased. As is known to those of ordinary skill in the art, if the programming charge stored in the memory cell is flipped by exposure to radiation, the state of the switching transistor cannot be guaranteed.

[0010] Accordingly, current memory cells must either be protected from the high-energy particle hit or designed in such a way that they are resistant to a change in data state even if hit by a high energy particle or exposed to a high energy EMP.

[0011] Hence, there is a need in the art for a transistor, memory cell, or circuit node that is resistant to a change in data state even if hit by a high energy particle or exposed to a high energy EMP. There is also a need in the art for a transistor, memory cell, or circuit node that has a reduced junction capacitance.

SUMMARY OF THE INVENTION

[0012] The present invention comprises a transistor device for an integrated circuit having a source, a drain and a gate. The transistor device also comprises a p-substrate level, an n-well layered on the p-substrate and a fully depleted p-well

4

layered on the n-well. The transistor device has a first N+ region layered on the

fully depleted p-well and a second N+ region layered on the fully depleted p-well.

The first N+ region is coupled to the drain of the transistor and the second N+

region layered on the P-well is coupled to the source.

[0013]   A better understanding of the features and advantages of the present

invention will be obtained by reference to the following detailed description of the

invention and accompanying drawings, which set forth an illustrative embodiment

in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]   FIG. 1 is a cross-sectional view of an illustrative n-channel

embodiment of a reduced-capacitance floating-gate transistor according to the

present invention.

[0015]   FIG. 2 shows the voltage potential in the bulk under the surface of

the transistor device according to FIG. 1 when it is biased at V_T.

[0016]   FIG. 3 is a cross-sectional view of an illustrative p-channel

embodiment of a reduced-capacitance floating-gate transistor according to the

present invention.

DETAILED DESCRIPTION

[0017] Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

[0018] FIG. 1 is a cross-sectional view of an n-channel floating-gate transistor 100 according to an illustrative embodiment of the present invention. Transistor 100 is formed on a p-type substrate 102. P-type substrate 102 may be doped to a level of about 1e18. An n-type region 104 is disposed above the substrate 102 and may be formed, for example, as an n-well doped to a level of about 1e18 or as a buried layer. A p-type region 106 is disposed above n-type region 104 and may also be formed as a well structure doped to a level of about 1e17. Those of ordinary skill in the art will appreciate that the doping levels will be process-generation dependent and will also be limited by the voltages to be used in the devices to avoid zener breakdown voltages close to the operating range.

[0019] N-type source and drain regions 108 and 110 are heavily doped and are disposed in the p-type region 106 and are spaced apart from one another to form a channel region 112. Floating gate 114, preferably formed from doped polysilicon as is known in the art, is disposed above and insulated from the

channel 112 and is self aligned with source and drain regions 108 and 110 as is known in the art. Control gate 116, also preferably formed from polysilicon, is disposed above and insulated from floating gate 114. While the embodiment depicted in FIG. 1 is a floating gate memory cell transistor, persons of ordinary skill in the art will readily observe that the principles of the present invention are equally applicable to standard, single-gate MOS transistors.

[0020]   An isolation trench 118 surrounds transistor 100 to isolate it from adjacent devices. FIG. 1 only shows the side portions of isolation trench 118; persons of ordinary skill in the art will recognize that portions of isolation trench 118 located in front of and behind the plane of the figure are not shown. A p-type implant may be made in trench 116 as shown in FIG. 1

[0021]   In transistor 100, p-type region 106 is fully depleted by reverse biasing the n-type region with respect to both it and the p-type substrate 102. As an illustrative example, in a device created with a 0.15 micron process, the sources and drains will have voltages of between about zero and 1.5 volts, n-type region 104 may be biased at about 3.3 volts. p-type region 106 may be charge-pump biased at about -2 to about -3 volts, and substrate 102 may be biased at about -3 volts. The punch through of n-type layer 104 to the source region 108 and drain region 110 is greater than 3.3 volts but is fully depleted by the approximately -3 volts on the substrate 102.   This serves to reduce the junction capacitance of the

transistor 100 because the junction between N+ drain region 108 and the fully depleted p-type region 106 has very little junction capacitance as compared with a standard transistor of the same generation without the fully depleted well. Persons of ordinary skill in the art will recognize that the bias voltages can readily be optimized for device-size scaling and different doping levels

[0022]   In addition, because of the punch trough of the n-type region 104 to the N+ source region 108 and drain region 110 and because p-type region 106 is fully depleted by the -3 volts on the buried p-type substrate layer 102, a field will sweep away any minority carriers to the n-type region 104, thus protecting the surface from being upset by a radiation pulse. Also, the transistor gamma is greatly reduced as change in charge of p-well 106 to the surface is small.

[0023]   Moreover, by using trench isolation the device field can be run into the substrate buried layer N+ thereby preventing lateral punch through. Thus, the only leakage that may be a concern for radiation hits is V_T drift and leakage at the channel-edge to field oxide boundary.

[0024]   According to one aspect of the invention, the n-type region 104 may be laid out in a grid formation to improve the impedance of minority carriers in depleted regions in order to avoid filling the wells with charge and thus changing the V_T of the device.

[0025] FIG. 2 shows the Fermi Level of a fully space-charge-depleted N-Channel transistor going vertically down into the substrate directly under the gate electrode. As can be seen at 0 microns the surface channel is biased at 0 volts as this device is in the on state (it could also be at Vcc). Continuing down into the substrate the fully depleted P-type silicon adds negative charge and therefore the voltage of the Fermi level goes negative until the field reverses direction at a depth of about 0.115u. At this point the field from the N+ region farther down causes the voltage to rise up to 3.3Volts as it reaches a depth of 0.3u, which is the N+ buried layer biased at 3.3Volts (the I/O voltage). Those familiar with CCD devices will recognize this as a depleted well device where the well reaches a minimum voltage of -1.1 volts. In this case it is desired to avoid filling the well with holes to avoid affecting the Vt of the transistor. Therefore there must be a more heavily doped p-type region near the end of the transistor gate field region which transfers the bias of the p-type substrate to the depleted well.

[0026] There are several ways to accomplish this. A p-type region can be formed around the isolation trench. This region should extend into the substrate. This is a normal technique used to prevent inversion problems under the field oxide.

[0027] There are other ways to accomplish this result. If a buried layer is used it can be terminated before the trench isolation to allow the trench p doping

reach the p-type substrate. Also if a triple well process employing a retrograde n-well is used then the p-well can be extended outside the n-well to reach the p substrate doping. This is also the purpose of the N+ buried layer in the p channel transistor. If a no-buried-layer scheme is used then n doping may be performed in the shallow trench. This doping must be connected to an n+ region at the surface which will be biased at a potential of Vcc plus the depletion voltage. In the present example, 3.3 volts would be fine. This allows the bias of the p-type substrate (e.g., -1.5 volts or more negative; it must be less than the minimum voltage of the depleted p-well) to connect to the depleted well to allow a path to remove holes that will slowly accumulate. Another point to observe is that the minimum voltage in the well must be at least 1/2 volt less than the surface channel to prevent electrons from going from the surface to the buried layer (commonly called punchthrough). In this example the p well is doped to 2e17 and the n+ buried layer is 1e19.

[0028]   FIG. 3 is a simplified cross-sectional view of an illustrative p-channel embodiment of a transistor having fully-depleted junctions according to the present invention. Transistor 200 Transistor is formed on a p-type substrate 202. P-type substrate 202 may be doped to a level of about 1e18. An n-type region 204 is disposed above the substrate 202 and may be formed, for example, as an n-well doped to a level of about 1e17 or as a buried layer. N-type buried layers 206 are disposed at about the boundary between substrate 202 and n-type region 204

and may be doped to a level of from about 1e18 to about 2e18. Those of ordinary skill in the art will appreciate that the doping levels will be process-generation dependent.

[0029]   P-type source and drain regions 208 and 210 are heavily doped and are disposed in the n-type region 204 and are spaced apart from one another to form a channel region 212. Floating gate 214, preferably formed from doped polysilicon as is known in the art, is disposed above and insulated from the channel 212 and is self aligned with source and drain regions 208 and 210 as is known in the art. Control gate 216, also preferably formed from polysilicon, is disposed above and insulated from floating gate 214. While the embodiment depicted in FIG. 3 is a floating gate memory cell transistor, persons of ordinary skill in the art will readily observe that the principles of the present invention are equally applicable to standard, single-gate p-channel MOS transistors.

[0030]   An isolation trench 218 surrounds transistor 200 to isolate it from adjacent devices. FIG. 3 only shows the side portions of isolation trench 218; persons of ordinary skill in the art will recognize that portions of isolation trench 218 located in front of and behind the plane of the figure are not shown.

[0031]   In transistor 200, n-type region 204 is fully depleted by reverse biasing the n-type buried layers with respect to both it and the p-type substrate

11

202. As an illustrative example, in a 0.15 micron process, the sources and drains will have voltages of between about zero and 1.5 volts, n-type region 204 may be biased at about 3.3 volts which may be supplied by biasing the n-type buried regions 206 at about 3.3 volts, and substrate 202 may be biased at about -3 volts as a result of biasing the integrated for the n-channel devices. The punch through of p-type substrate layer 202 to the source region 208 and drain region 210 is greater than 3.3 volts but is fully depleted by the approximately +3 volts on the n+/n regions 206 and 204. This serves to reduce the junction capacitance of the transistor 200 because the junction between source region 208 and drain region 210 and the fully depleted n-type region 2046 has very little junction capacitance. Persons of ordinary skill in the art will recognize that the bias voltages can readily be optimized for device-size scaling and different doping levels.

[0032]   In addition, because of the punch through of the p-type substrate 202 to the p+ source region 208 and drain region 210 and because n-type region 204 is fully depleted by the +3 volts on the n-type region 204, a field will sweep away any minority carriers to the n-type region 206, thus protecting the surface from being upset by a radiation pulse. Also, the transistor gamma is greatly reduced as change in charge between the n region 206 and the surface is small.

[0033]   Moreover, by using trench isolation the device field can be run into the substrate buried layer N+ thereby preventing lateral punch through. Thus, the

only leakage that may be a concern for radiation hits is V_T drift and leakage at the channel-edge to field oxide boundary.

[0034]   The transistor 200 of FIG 3 is advantageously employed in a CMOS process where devices such as the transistor 100 of FIG. 1 having a buried layer as n-type region 104 are employed. The same mask may be used to form n-type buried region 104 in transistor 100 of FIG. 1 and n-type buried layers 206 of FIG. 3.

[0035]   As will be appreciated by persons of ordinary skill in the art, the charge collection from a heavy ion hit is usually collected in the n-channel devices fabricated on the substrate whereas p-channel devices can only collect charge from the shallow n-well in which they are formed. This means that the critical charge collection on the p-channel devices is considerably less. If a designer decides that the p- channel devices do not need shielding then this scheme only needs to be done on the n-channel transistors. Since foundries are presently offering triple-well in a 90 nm process, practice of the present invention is facilitated.

[0036]   As will be well understood by those of ordinary skill in the art having the benefit of this disclosure, the voltages used in the above example can

be varied considerably by changing the dopings and spacings of the various layers of the structure.

[0037]   It should be understood that various alternatives to the embodiments of the disclosed method and apparatus described herein maybe employed in practicing the disclosed method and using the disclosed apparatus. It is intended that the following claims define the scope of the disclosed method and apparatus and that methods and structures within the scope of these claims and their equivalents be covered thereby.